A Highly Efficient and Reliable Inverter Configuration Based Cascaded Multilevel Inverter for PV Systems

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***Abstract*—This paper presents an improved cascaded multilevel inverter (CMLI) based on a highly efficient and reliable configuration for the minimization of the leakage current. Apart from a reduced switch count, the proposed scheme has additional features of low switching and conduction losses. The proposed topology with the given pulse width modulation (PWM) technique reduces the high-frequency voltage transitions in the terminal and common-mode voltages. Avoiding high-frequency voltage transitions achieves the minimization of the leakage current and reduction in the size of electromagnetic interference filters. Furthermore, the extension of the proposed CMLI along with the PWM technique for $2m+1$ levels is also presented, where m represents the number of photovoltaic (PV) sources. The proposed PWM technique requires only a single carrier wave for all $2m+1$ levels of operation. The total harmonic distortion of the grid current for the proposed CMLI meets the requirements of IEEE 1547 standard. A comparison of the proposed CMLI with the existing PV multilevel inverter topologies is also presented in the paper. Complete details of the analysis of PV terminal and common-mode voltages of the proposed CMLI using switching function concept, simulations, and experimental results are presented in the paper.**

***Index Terms*—Cascaded multilevel inverter (CMLI), common-mode voltage (CMV), leakage current, terminal voltage.**

I. Introduction

TRANSFORMERLESS multilevel inverter (MLI) topologies are gaining importance due to their advantages such as high efficiency, low switch count, low weight, and reduced size. However, removal of the transformer eliminates the galvanic isolation between the photovoltaic (PV) array and the output load. Removal of galvanic isolation increases the leakage current compromising the safety in PV systems. It has led to the development of various safety standards for the PV systems, which restrict the value or magnitude of leakage current flow in the PV system [1]–[5]. Apart from leakage current minimization, there is a continuously increasing demand for high-quality power output to be fed into the grid from the PV system. This requirement has led to the use of MLI in the transformerless PV systems. In the literature, many topologies or configurations of MLIs [6], [7] are proposed for the minimization of leakage current for their application in the transformerless PV systems. These configurations employ two methods for minimization of the leakage current [8]. One method is based on maintaining the common-mode voltage (CMV) constant, while the other method is based on the minimization of the high-frequency transitions in the terminal and CMVs.

One elegant solution based on maintaining a constant CMV is proposed by Zhang *et al.* [9]. The given MLI configuration [9] consists of eight switches for the generation of three levels in the output voltage. This topology reduces the switching losses but has the drawback of high conduction losses during both turn-ON and zero voltage states. The given MLI configuration has an asymmetric operation during each half-cycle of the fundamental component of the grid voltage. The inherent asymmetry in each half-cycle causes a dc offset in the MLI output voltage. Furthermore, the requirement of an additional number of switches for more than three-level operation limits its application. Islam and Mekhilef [10] have proposed another interesting transformerless PV MLI topology to reduce the leakage current by maintaining CMV constant. This MLI topology uses six switches for the generation of three levels in the inverter output voltage. This circuit configuration results in high switching and conduction losses. Furthermore, this MLI topology cannot be extended to more than three levels in the output voltage. Xiao *et al.* [11] have proposed another efficient three-level MLI for the minimization of leakage current by maintaining CMV constant. The given topology [11] has low conduction and switching losses. However, this configuration suffers from the disadvantage of a high number of device count. Another interesting topology with low switching losses based on constant CMV is proposed by Ji *et al.* [12]. This MLI topology consists of six switches and two diodes. Apart from resulting in high conduction losses, this topology is less amenable for an extension to a higher number of levels in the output voltage.

Another important method to minimize the leakage current is by the elimination of high-frequency voltage transitions in the CMV. One such interesting solution is proposed by Buticchi *et al.* [13]. The authors have proposed a nine-level grid-tied PV MLI topology. This MLI topology consists of eleven switches and four diodes. In this MLI, four switches in the low-voltage

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bridge are operated with high switching frequency, while the remaining switches in the high-voltage bridge are operated with the low switching frequency. For a proper operation of this configuration [13], the balance of flying capacitor voltage $V_{\rm fc}$ is necessary. Furthermore, the PV terminals in this MLI topology cannot be grounded. Based on a similar concept, another good proposal is given by Hong *et al*. [14]. In this solution, the authors have proposed a single inductor dual buck full-bridge inverter for the generation of variable CMV at low frequency. The MLI topology requires six switches and two diodes. The switches in the H-bridge are operated at a low switching frequency, while the bidirectional switch is operated at a high switching frequency. However, details of extending the topology for a higher number of levels are not explained in the paper [14].

From the above-mentioned discussion, it is evident that there is a need for a generalized transformerless PV MLI, with fewer semiconductor devices to achieve the objectives of high efficiency and economy. It should also be ensured that the PV MLI should have its switching and conduction losses optimized with a lower number of conducting switches during the zero voltage state. Furthermore, the extension to the higher number of levels should be possible. This paper proposes one such solution for the minimization of leakage current in transformerless MLIs connected to PV systems. The pulse width modulation (PWM) technique for the proposed MLI is also discussed in the paper. The analysis of PV terminal and CMVs using switching function is presented. This analysis leads to the development of the proposed PWM technique, which prevents high-frequency voltage transitions in the terminal voltage and CMV. Salient features of the proposed cascaded MLI (CMLI) are as follows.

1) The topology uses eight switches for the generation of five levels in the output voltage.
2) During the zero voltage state only one switch and one diode conduct.
3) In the proposed topology, four switches are operated at a low switching frequency, which reduces the switching losses.
4) The dead band in the PWM technique does not affect the CMV.
5) The proposed inverter can be easily cascaded to achieve more than five levels in the output.

Rest of the paper is organized into eight sections. Section II describes the working principle and the operation for the proposed five-level grid-connected CMLI along with the generalized structure. The details of the PWM technique employed with its generalization for $2m + 1$ levels are explained in Section III. Section IV gives the details of the maximum power point tracking (MPPT) algorithm which can be applied to the proposed five-level CMLI. This is followed by the analysis of terminal and CMVs for the proposed CMLI in Section V. Section VI discusses the simulation results of the proposed five-level grid-connected CMLI. Section VII shows the experimental results of the proposed five-level and nine-level CMLI. Comparison of the proposed CMLI with the other existing PV MLI topologies in the literature is presented in Section VIII. The conclusions from the paper are discussed in Section IX.

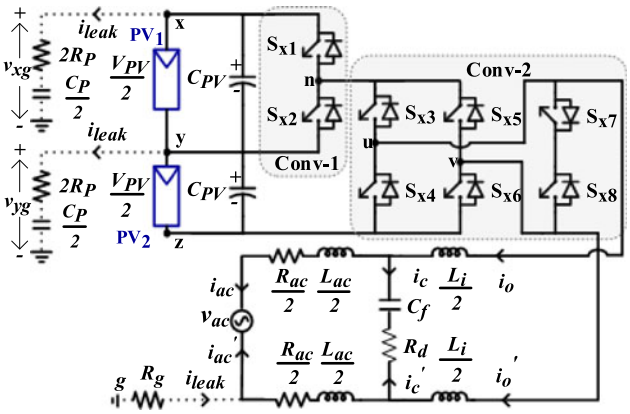

Fig. 1. Proposed five-level grid-connected CMLI with PV and parasitic elements.

II. Operation of the Proposed Cascaded Five-Level MLI

The schematic circuit diagram of the proposed five-level CMLI for the PV system is shown in Fig. 1. The given configuration consists of two converters (Conv-1 and Conv-2). Conv-1 is a half-bridge inverter comprising two switches S_{x1} and S_{x2}. The Conv-2 comprises of a highly efficient and reliable inverter configuration [15] with six switches (S_{x3}–S_{x8}). Among the six switches, four switches (S_{x3}–S_{x6}) in Conv-2 constitute an H-bridge circuit. The remaining two switches $S_{\rm x7}$ and S_{x8} in Conv-2 are bidirectional switches. The switches in the Conv-1 are used to generate the voltage levels of $V_{\rm PV}$ and $V_{\rm PV}/2$. When switch S_{x1} is turned ON, the voltage $V_{\rm PV}$ is applied at the terminal n with respect to the terminal z. Similarly, the terminal n attains the voltage $V_{\rm PV}/2$ when switch S_{x2} is turned ON. The switches S_{x1} and S_{x2} are complementary in nature. The generated voltage levels at the terminal n of Conv-1 are given as an input to the Conv-2. The Conv-2 generates the positive, negative, and zero levels of corresponding input voltage (voltage between the terminals n and z) across the load. The bidirectional switches S_{x7} and S_{x8} provide the free-wheeling path during zero voltage state. The output of the five-level CMLI is connected to the grid through an *LCL* filter as shown in Fig. 1 [16]–[18]. It consists of inverter side inductance L_i, capacitance C_f, and grid side inductance $L_{\rm ac}$. The resistance R_d in the shunt branch of the filter is used as a damping resistor. The resistance $R_{\rm ac}$ refers to the grid side resistance, and the resistance R_g indicates resistance in the ground path. The variable $v_{\rm ac}$ refers to instantaneous grid voltage. The variables R_p and C_p refer to the parasitic resistance and capacitance in the PV system, respectively, shown with dotted lines in Fig. 1. The parasitic capacitance in the PV system forms a resonant circuit with the filter inductances [16]. The variables i_o, i_c, and $i_{\rm ac}$ denote the output current of the five-level CMLI, current flowing through shunt branch of the filter, and the current flowing into the grid, respectively. The current $i_{\rm leak}$ indicates the leakage current flowing from the PV array into the ground through parasitic capacitance (see Fig. 1).

The proposed MLI topology contains four pairs of complementary switches (S_{x1}, S_{x2}), (S_{x3}, S_{x4}), (S_{x5}, S_{x6}), and (S_{x7},

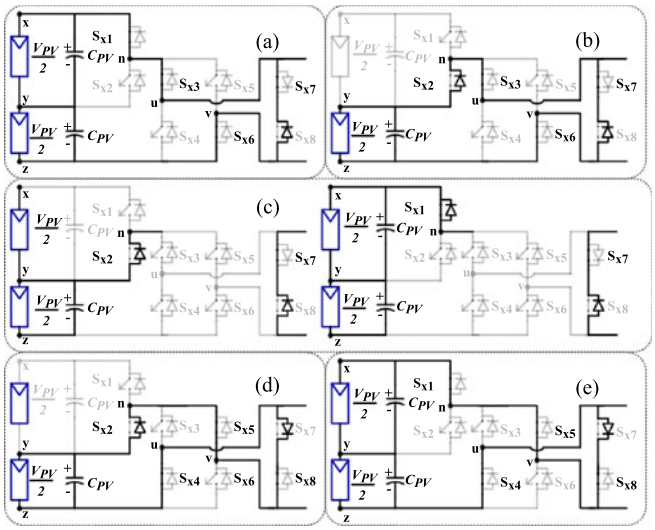

Fig. 2. Single-phase five-level cascaded MLI for output voltage levels (a) $+V_{\mathrm{PV}}$, (b) $+V_{\mathrm{PV}}/2$, (c) 0, (d) $-V_{\mathrm{PV}}/2$, and (e) $-V_{\mathrm{PV}}$.

TABLE I
SWITCHING STATES WITH THEIR RESPECTIVE OUTPUT VOLTAGE

S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	S_{x7}	S_{x8}	v_{uv}
1	0	1	0	0	1	1	0	$+V_{\mathrm{PV}}$
0	1	1	0	0	1	1	0	$+V_{\mathrm{PV}}/2$
0	1	0	0	0	0	1	0	0
1	0	0	0	0	0	1	0	0
0	1	0	1	1	0	0	1	$-V_{\mathrm{PV}}/2$
1	0	0	1	1	0	0	1	$-V_{\mathrm{PV}}$

S_{x8}) in the proposed configuration. However, to minimize the leakage current, the complementary switching is employed only for the two pairs of switches (S_{x1}, S_{x2}) and (S_{x7}, S_{x8}). Avoiding complementary action for the other pairs of switches helps in isolating the PV and the grid source during the zero voltage state.

Fig. 2 shows the operation of the inverter in all its switching states. The inverter output voltage v_{uv} at different voltage levels with the corresponding switching states of all the switches is shown in Table I. The inverter output voltage v_{uv} attains the voltage levels $+V_{\mathrm{PV}}$ or $-V_{\mathrm{PV}}$ when switch S_{x1} is turned ON along with other inverter switches (S_{x3}, S_{x6}) or (S_{x4}, S_{x5}), respectively, as shown in Fig. 2(a) and (e). Similarly, the voltage levels $+V_{\mathrm{PV}}/2$ or $-V_{\mathrm{PV}}/2$ are obtained at v_{uv} when switch S_{x2} is turned ON with the same switching combinations as shown in Fig. 2(b) and (d). The most important feature to be noticed during zero voltage state or free-wheeling stage is the isolation or disconnection between PV source and the grid. The isolation between the PV source and the grid can be achieved by turning OFF all the switches of the H-bridge inverter as shown in Fig. 2(c).

The turn-OFF state of four switches in H-bridge during the zero voltage state results in the isolation of PV source from the grid. The bidirectional switches S_{x7} and S_{x8} provide a free-wheeling path for the inductor current during the turn-OFF period of a switching cycle. This action helps in minimizing the

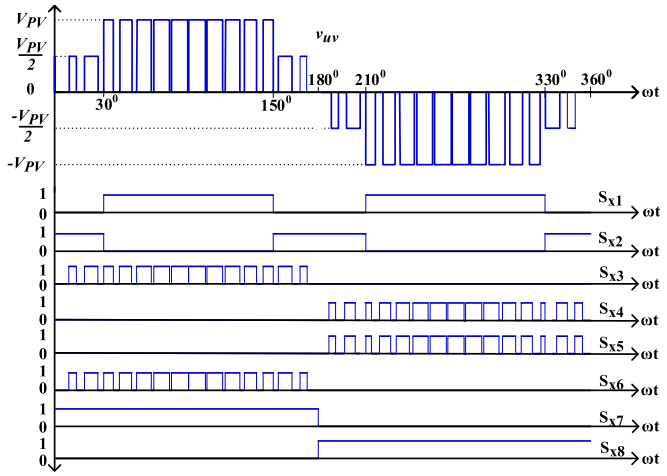

Fig. 3. Gate pulses for the switches corresponding to inverter output voltage.

leakage current flowing through the parasitic capacitance. As there is no direct connection between the two sources, the PV terminal points (nodes x, y, and z) float and have undefined voltages. The float or undefined value restricts the terminal voltages from becoming zero. Thus, high-frequency voltage transitions at the PV terminals are avoided. In other words, the possibility of the flow of leakage current can be minimized. Also, in the other intermediate states such as switching between $V_{\mathrm{PV}}/2$ to V_{PV} or vice-versa, again the same principle can be used. The above action further helps in the minimization of the leakage current in the PV system. The PWM technique for the proposed five-level CMLI is broadly discussed in Section III. The expressions for the pole voltages v_{uz} and v_{vz} is given, respectively, as

$$v_{\mathrm{uz}} = \left(S_1 S_3 + 0.5 S_2 S_3 - \frac{1}{(S_3+S_4)} + \frac{1}{(S_3+S_4)(S_1+S_2)}\right) V_{\mathrm{PV}} \tag{1}$$

$$v_{\mathrm{vz}} = \left(S_1 S_5 + 0.5 S_2 S_5 - \frac{1}{(S_5+S_6)} + \frac{1}{(S_5+S_6)(S_1+S_2)}\right) V_{\mathrm{PV}} \tag{2}$$

where S_a ($a = 1, 2, 3, \ldots$) is the switching state of switch S_{xa} whose value can be either 1 (stands for turn-ON) or 0 (stands for turn-OFF).

Fig. 3 shows the switching pattern of all the switches for the corresponding inverter output voltage v_{uv}. The switches S_{x1} and S_{x2} in the half-bridge are operated at low switching frequency. In order to eliminate the high switching frequency operation, the switch S_{x2} is kept turned ON in the zero state during voltage transition between the levels 0 to $V_{\mathrm{PV}}/2$. Similarly, the switch S_{x1} is kept turned ON, during voltage transition between levels 0 to V_{PV}. The inverter switch pair (S_{x3}, S_{x6}) is operated with a high switching frequency during positive half-cycle, and it remains at the turn-OFF state during the negative half-cycle of the inverter output voltage v_{uv}. A similar operation is applicable

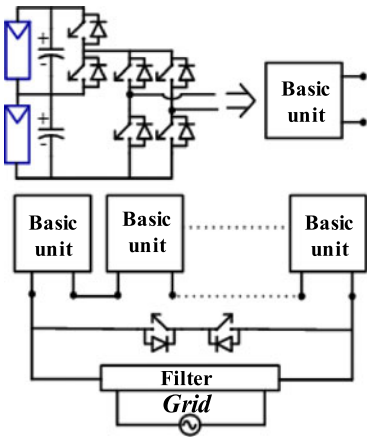

Fig. 4. Generalized $2m + 1$ level MLI topology derived from the proposed five-level CMLI.

to the other inverter switch pair (S_{x4}, S_{x5}), which is operated with higher switching frequency during the negative half-cycle.

The switches S_{x7} and S_{x8} are turned ON during positive and negative half-cycles of the output voltage $v_{\rm uv}$, respectively. The removal of complementary action from the pair of switches (S_{x3}, S_{x4}) and (S_{x5}, S_{x6}) facilitates complete turn-OFF of the switches during each half-cycle of the output voltage $v_{\rm uv}$. Thus, the proposed system has the advantage of reduced switching losses, realizing to a highly efficient and reliable inverter configuration which may result in higher efficiency.

The generalized topology for $2m + 1$ levels can also be obtained for the proposed five-level CMLI. The number of PV sources in the CMLI is denoted by the term m. The value of m is always an integral multiple of 2 (i.e., $m = 2, 4, \ldots$). The extended version of the proposed CMLI for $2m + 1$ levels is presented in Fig. 4. The generalized topology is obtained by cascading the basic units consisting of half-bridge and H-bridge. The bidirectional switches are connected in between the output terminals for the free-wheeling period. The proposed generalized $2m + 1$ level MLI is also compared with the half-bridge and full-bridge modular multilevel converter. The half-bridge modular multilevel converter requires less number of switches when compared to the proposed generalized $2m + 1$ level MLI. However, it is difficult to reduce or minimize the flow of leakage current in the half-bridge modular multilevel converter. Also, the number of electrolytic capacitors used at the input side of the half-bridge modular multilevel converter is high compared to the proposed generalized $2m + 1$ level MLI. The proposed MLI has a lesser device count when compared to the full-bridge modular multilevel converter [19]. However, both can minimize the leakage current flowing through the PV system.

III. Proposed PWM Strategy Along With Generalized Strategy for Minimization of the Leakage Current

The operation of the proposed PWM technique is explained by considering the given five-level CMLI. The high-frequency transitions in the terminal voltages $v_{\rm xg}$ and $v_{\rm yg}$ of the five-level

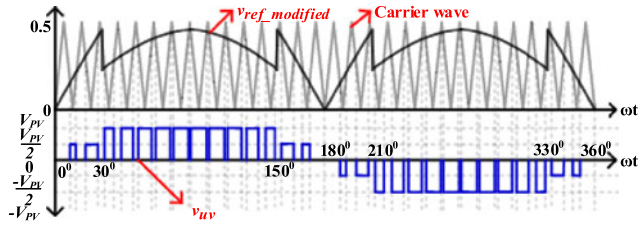

Fig. 5. Waveform of output voltage $v_{\rm uv}$ for the proposed PWM technique.

CMLI are minimized using the proposed PWM technique. The suggested action can be achieved by switching from $V_{\rm PV}$ to 0 state or vice-versa instead of the switching from $V_{\rm PV}$ to $V_{\rm PV}/2$ state or vice-versa. Additionally, during the zero voltage state or free-wheeling period of the switching cycle, the PV array is isolated from the grid. The isolation of the PV array and the grid during zero voltage state is similar to the inverter configuration reported in [15]. The magnitude of reference wave $v_{\rm mod}$ is lowered to 50% of its original value whenever the switching is toggled amongst the levels $V_{\rm PV}$ and 0. The above action is mainly done to accommodate the value of PV voltage $V_{\rm PV}$. The modification in the value of $v_{\rm mod}$ is done whenever the instantaneous magnitude of modulating wave $v_{\rm mod}$ exceeds the value of $m_a/2$, where m_a refers to the modulation index. By incorporating the desired modification, the output voltage includes the zero voltage state (i.e., free-wheeling state) in all its switching periods. The expression for modified reference waveform $v_{\rm ref\_modified}$ is given as

$$v_{\rm ref\_modified} = \begin{cases} v_{\rm mod} & \text{for} \quad 0 \le |v_{\rm mod}| < \frac{m_a}{2} \quad \text{from} \quad \frac{V_{\rm PV}}{2} \quad \text{to} \quad 0 \\ \frac{v_{\rm mod}}{2} & \text{for} \quad \frac{m_a}{2} \le |v_{\rm mod}| < m_a \quad \text{from} \quad V_{\rm PV} \quad \text{to} \quad 0 \end{cases} \tag{3}$$

where $v_{\rm mod} = m_a \sin\omega t$ gives the magnitude of $v_{\rm mod}$.

The output voltage of the proposed PWM technique for the five-level CMLI is shown in Fig. 5. In Fig. 5, the modified reference wave is compared with the triangular carrier wave. During the positive half-cycle of voltage $v_{\rm ac}$, whenever the phase angle ωt lies in range 0–30° and the instantaneous magnitude of $v_{\rm ref\_modified}$ exceeds the carrier wave, then $v_{\rm uv}$ attains the voltage level of $V_{\rm PV}/2$ otherwise, it is switched to the zero voltage state. Similarly, when ωt lies in the range 30–150°, the inverter output voltage $v_{\rm uv}$ attains the voltage level of $V_{\rm PV}$ whenever the instantaneous magnitude $v_{\rm ref\_modified}$ exceeds the carrier wave or attains zero value otherwise. In the same positive half-cycle, for the remaining range of ωt (i.e., between 150° and 180°), $v_{\rm uv}$ attains the voltage levels $V_{\rm PV}/2$ if the instantaneous magnitude of $v_{\rm ref\_modified}$ is greater than the carrier wave. A similar sequence is adopted during the negative half-cycle of voltage $v_{\rm ac}$. Thus, in the complete cycle if the magnitude of $v_{\rm ref\_modified}$ is less than the carrier wave, then $v_{\rm uv}$ attains zero voltage level.

For the implementation of the proposed PWM to a $2m + 1$ level inverter, the waveform of generalized modified reference wave $v_{\rm ref\_modified\_gen}$ is shown in Fig. 6. The term m refers to the number of PV sources used. Whenever the instantaneous

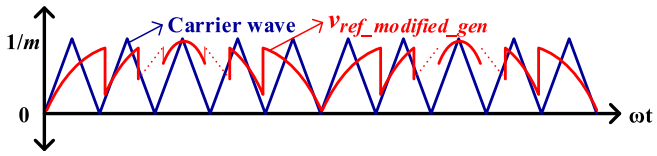

Fig. 6. Waveform of generalized modified reference wave $v_{\text{ref\_modified\_gen}}$.

absolute magnitude of v_{mod} exceeds the value $j(m_a/m)$, the magnitude of $v_{\text{ref\_modified\_gen}}$ becomes $k(|v_{\text{mod}}|/m)$ where $j = 1, 2, \ldots, m$–1, m and $k = 1, 2, \ldots, m$–1. The expression for $v_{\text{ref\_modified\_gen}}$ is given as

$$v_{\text{ref\_modified\_gen}} = \begin{cases} v_{\text{mod}} & \text{for} \quad 0 \le |v_{\text{mod}}| < \frac{m_a}{m} \quad \text{from} \quad \frac{V_{\text{PV}}}{m} \text{to} \quad 0 \\ \frac{v_{\text{mod}}}{2} & \text{for} \quad \frac{m_a}{m} \le |v_{\text{mod}}| < \frac{2m_a}{m} \quad \text{from} \quad \frac{2V_{\text{PV}}}{m} \text{to} \quad 0 \\ \vdots & \\ \frac{v_{\text{mod}}}{m} & \text{for} \quad \frac{(m-1)m_a}{m} \le |v_{\text{mod}}| < m_a \quad \text{from} \quad V_{\text{PV}} \text{to} \quad 0 \end{cases}. \tag{4}$$

IV. Integration of MPPT for the Proposed Five-Level CMLI

The well-known perturb and observe algorithm [20] is employed for the two PV sources (considering five-level operation) individually to track maximum power point (MPP). Thus, each MPPT algorithm tracks the MPP for respective PV sources. To track the MPP, the required information of 1) the average values of the two PV source voltages (V_{PV1} and V_{PV2} for the PV sources PV_1 and PV_2, respectively) and 2) the currents (I_{PV1} and I_{PV2} for the PV sources PV_1 and PV_2, respectively) are sensed and then given to their respective MPPT algorithms. The MPPT algorithms then use the sensed values of the PV voltages and currents for the calculation of the individual values of the modulation indices m_{a1} and m_{a2} for the two PV sources PV_1 and PV_2, respectively. The outputs of two MPPT algorithms are then utilized for the calculation of overall modulation index m_a. The expression for m_a is given as

$$m_a = m_{a1}\frac{V_{\text{PV1}}}{V_{\text{PV1}} + V_{\text{PV2}}} + m_{a2}\frac{V_{\text{PV2}}}{V_{\text{PV1}} + V_{\text{PV2}}}. \tag{5}$$

The calculated modulation index m_a is then used by the PWM strategy as described in the above-mentioned section to generate the PWM pulses for the proposed five-level CMLI.

V. Analytical Expressions of PV Terminal Voltage and Common-Mode Voltage for the Proposed Cascaded Five-Level Inverter

The analysis of the leakage current can be carried out from the expression of terminal voltages v_{xg}, v_{yg}, and v_{zg}. The expression for the PV terminal voltages can be derived from the switching function analysis [21]. From Fig. 1, using the superposition theorem, the PV terminal voltages v_{xg} and v_{yg} are expressed as follows:

$$v_{\text{xg}} = S_1 v_{x1g} + S_2 v_{x2g} \tag{6}$$

$$v_{\text{yg}} = S_1 v_{y1g} + S_2 v_{y2g}. \tag{7}$$

The terms v_{x1g} and v_{y1g} are the voltages at terminals x and y, respectively, when switch S_{x1} is turned ON. Similarly, v_{x2g} and v_{y2g} are the voltages at terminals x and y, respectively, when switch S_{x2} is turned ON.

The expression for the voltage v_{zg} when switch S_{x1} is turned ON is given as

$$v_{\text{zg}} = v_{x1g} - V_{\text{PV}}. \tag{8}$$

Similarly, the expression for terminal voltage v_{zg} when switch S_{x2} is turned ON is given as

$$v_{\text{zg}} = v_{y2g} - \frac{V_{\text{PV}}}{2}. \tag{9}$$

With the use of the switching function analysis, the voltages v_{ug} and v_{vg} (from Figs. 1 and 2) expressed in terms of v_{x1g} and v_{zg} are shown, respectively, as

$$v_{\text{ug}} = S_1 S_3 v_{x1g} + S_4 v_{\text{zg}} \tag{10}$$

$$v_{\text{vg}} = S_1 S_5 v_{x1g} + S_6 v_{\text{zg}}. \tag{11}$$

Similarly, the voltages v_{ug} and v_{vg} (from Figs. 1 and 2) expressed in terms of v_{y2g} and v_{zg} using switching functions are shown, respectively, as

$$v_{\text{ug}} = S_2 S_3 v_{y2g} + S_4 v_{\text{zg}} \tag{12}$$

$$v_{\text{vg}} = S_2 S_5 v_{y2g} + S_6 v_{\text{zg}}. \tag{13}$$

Now expressing the voltages v_{ug} and v_{vg} in terms of the grid voltage v_{ac}, the voltage drop in filter inductors (L_i and L_{ac}) and resistances (R_{ac} and R_g) [21] can be given by

$$v_{\text{ug}} = \frac{L_i}{2}\frac{di_o}{dt} + \frac{L_{\text{ac}}}{2}\frac{di_{\text{ac}}}{dt} + v_{\text{ac}} + \frac{R_{\text{ac}}}{2}i_{\text{ac}} - R_g i_{\text{leak}} \tag{14}$$

$$v_{\text{vg}} = \frac{L_i}{2}\frac{di_o\prime}{dt} + \frac{L_{\text{ac}}}{2}\frac{di_{\text{ac}}\prime}{dt} + \frac{R_{\text{ac}}}{2}i_{\text{ac}}\prime - \text{R}_g i_{\text{leak}}. \tag{15}$$

Now, with the addition of (14) and (15), and by ignoring the voltage drop in resistances R_g and $R_{\text{ac}}/2$ with assumptions of $i_{\text{ac}} = -i'_{\text{ac}}$ and $i_o = -i'_o$, [21] gives

$$v_{\text{ug}} + v_{\text{vg}} = v_{\text{ac}}. \tag{16}$$

Substituting the values of v_{ug} and v_{vg} from (10) and (11) into (16) and simplifying those using (8) gives the expression for the terminal voltage v_{x1g} as

$$v_{x1g} = \frac{v_{\text{ac}} + V_{\text{PV}}(S_4 + S_6)}{(S_1 S_3 + S_1 S_5 + S_4 + S_6)}. \tag{17}$$

Now, the other terminal voltage v_{y1g} (when switch S_{x1} is ON) can be calculated by subtracting v_{x1g} and $V_{\text{PV}}/2$.

Similarly, substituting (12) and (13) into (16) and simplifying for terminal voltage v_{y2g} using (9) results in

$$v_{y2g} = \frac{v_{\text{ac}} + \frac{V_{\text{PV}}}{2}(S_4 + S_6)}{(S_2 S_3 + S_2 S_5 + S_4 + S_6)}. \tag{18}$$

TABLE II
VALUES OF COMMON-MODE VOLTAGE AND POLE VOLTAGES FOR CORRESPONDING OUTPUT VOLTAGE

v_{uv}	v_{uz}	v_{vz}	v_{cm}
$+V_{PV}$	V_{PV}	0	$V_{PV}/2$
$+V_{PV}/2$	$V_{PV}/2$	0	$V_{PV}/4$
0	Undefined	Undefined	Undefined
$-V_{PV}/2$	0	$V_{PV}/2$	$V_{PV}/4$
$-V_{PV}$	0	V_{PV}	$V_{PV}/2$

The other terminal voltage v_{x2g} can be calculated by adding v_{y2g} and $V_{PV}/2$. Now by using (6) and (7), the complete expression for terminal voltages v_{xg} and v_{yg} is given, respectively, as

$$v_{xg} = v_{ac}S_{W1} + V_{PV}S_{W2} + v_{ac}S_{W3} + \frac{V_{PV}}{2}S_{W4} + \frac{V_{PV}}{2}S_2 \quad (19)$$

$$v_{yg} = v_{ac}S_{W1} + V_{PV}S_{W2} + v_{ac}S_{W3} + \frac{V_{PV}}{2}S_{W4} - \frac{V_{PV}}{2}S_1. \quad (20)$$

The terms S_{W1}, S_{W2}, S_{W3}, and S_{W4} in (19) and (20) are given by

$$S_{W1} = \frac{S_1}{(S_1S_3 + S_1S_5 + S_4 + S_6)}$$

$$S_{W2} = \frac{S_1(S_4 + S_6)}{(S_1S_3 + S_1S_5 + S_4 + S_6)}$$

$$S_{W3} = \frac{S_2}{(S_2S_3 + S_2S_5 + S_4 + S_6)}$$

$$S_{W4} = \frac{S_2(S_4 + S_6)}{(S_2S_3 + S_2S_5 + S_4 + S_6)}.$$

Substituting the values $S_3 = 0, S_4 = 0, S_5 = 0$, and $S_6 = 0$ in the voltage state results in undefined value $(0/0)$ in the terminal voltages v_{xg}, v_{yg}, and v_{zg}. The undefined value $(0/0)$ during a zero voltage state is mainly because of isolating the PV source and grid. The isolation of PV source and grid can also be observed in Fig. 2(c). The CMV v_{cm} is obtained by taking the average of pole voltage v_{uz} and v_{vz} given in (1) and (2), respectively. The expression for v_{cm} is

$$v_{cm} = \left((S_1 + 0.5S_2)(S_3 + S_5) + \left(\frac{1}{(S_3 + S_4)} + \frac{1}{(S_5 + S_6)}\right) \times \left(\frac{1}{(S_1 + S_2)} - 1\right)\right)\frac{V_{PV}}{2}. \quad (21)$$

Table II gives the values of pole voltages (v_{uz}, v_{vz}) and CMV v_{cm} at different levels in the output voltage v_{uv}. During the turn-OFF period in a switching cycle, all the switches in the H-bridge are in a cut-off state so that the switching states S_3, S_4, S_5, and S_6 are equal to zero value. Substituting the corresponding values of S_3, S_4, S_5, and S_6 in (21) results in an undefined value (i.e., $v_{cm} = 0/0$) during the zero voltage state. The CMV attains the value $V_{PV}/2$ for both positive and negative levels of output voltage V_{PV} and attains the value $V_{PV}/4$ for both positive and negative levels of output voltage $V_{PV}/2$.

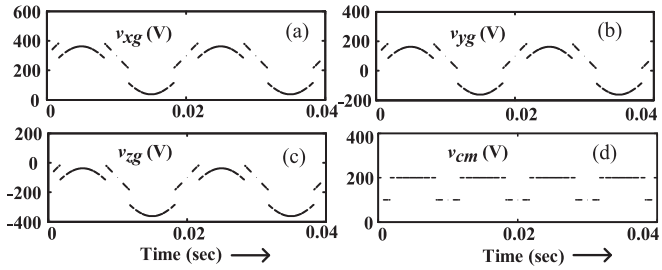

Fig. 7. Analytical results of the proposed five-level CMLI showing the waveforms of (a) terminal voltage v_{xg}; (b) terminal voltage v_{yg}; (c) terminal voltage v_{zg}; and (d) common-mode voltage v_{cm}.

TABLE III
PARAMETERS CONSIDERED FOR THE SIMULATION OF PROPOSED FIVE-LEVEL CMLI

Parameter	P	V_{dc}	f_{sw}	v_{ac}	f_{ac}
Value	2.5 kW	400 V	25 kHz	220 V	50 Hz
Parameter	L_{ac}	R_{ac}	R_g	L_i	C_f
Value	4 mH	0.01 Ω	0.1 Ω	4 mH	0.1 μF
Parameter	R_d	C_p	R_p		
Value	50 mΩ	200 nF	1 Ω		

The expressions for terminal and CMVs can be verified with MATLAB software using simulink block-set. The parameters $V_{PV} = 400$ V, switching frequency of the carrier wave $f_{sw} = 1$ kHz, $v_{ac} = 220$ V (rms), and the grid frequency $f_g = 50$ Hz are considered for the simulation. The carrier wave frequency is restricted to 1 kHz. This is done to demonstrate the undefined states clearly. Fig. 7 shows the waveforms of terminal voltages v_{xg}, v_{yg}, v_{zg}, and CMV v_{cm}. The discontinuity in the waveforms occurs when the PV source and grid are isolated. The isolation of grid and PV array results in an undefined value in the terminal and CMVs (discontinuity in the waveform). Since the value of the terminal and CMVs is undefined during the zero voltage state, they can be assumed to be restricted to the previous value. Thus, transitions in the voltage waveform can be minimized. In other words, it results in minimizing the high-frequency voltage transitions in the terminal and CMVs. Minimization or reduction of high-frequency voltage transitions in the terminal voltage further helps in reducing the leakage current in the PV system. The PV array parasitic capacitance [18] offers a high impedance for the low-frequency transitions in the terminal voltage. Thus, the magnitude of leakage current flowing through the parasitic capacitance is less. In other words, the proposed PWM technique minimizes the leakage current by reducing the high-frequency transitions in the terminal and CMVs.

VI. SIMULATION RESULTS

To support the switching function analysis given in the previous section, the proposed five-level CMLI is simulated using POWERSIM blocks in the MATLAB/SIMULINK software. The PWM technique explained in Section III is used for the

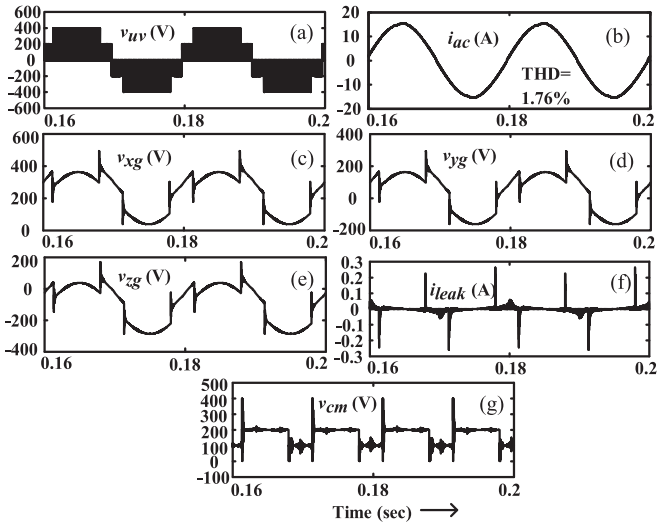

Fig. 8. Simulation results of the proposed five-level CMLI showing the waveforms of (a) output voltage $v_{\rm uv}$; (b) grid current $i_{\rm ac}$; (c) terminal voltage $v_{\rm xg}$; (d) terminal voltage $v_{\rm yg}$; (e) terminal voltage $v_{\rm zg}$; (f) leakage current $i_{\rm leak}$; and (g) common-mode voltage $v_{\rm cm}$.

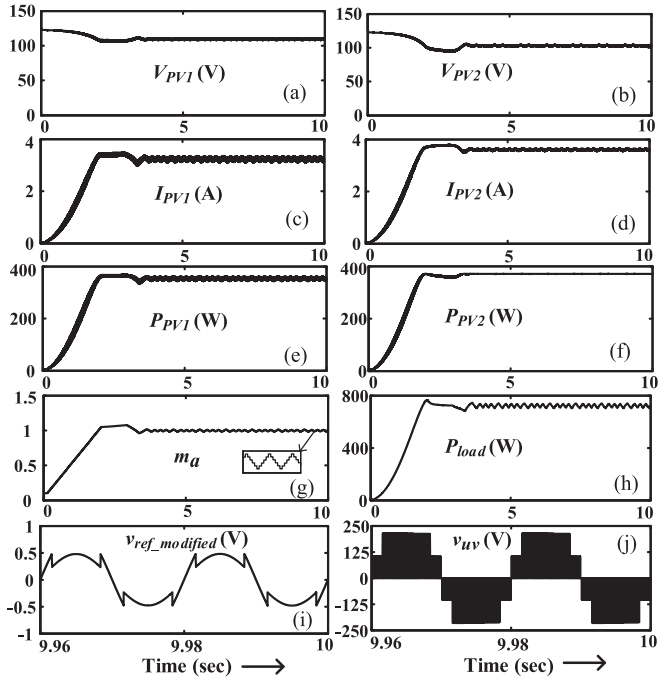

Fig. 9. Proposed five-level CMLI integrated with MPPT. The subplots give waveforms of (a) voltage $V_{\rm PV1}$; (b) voltage $V_{\rm PV2}$; (c) current $I_{\rm PV1}$; (d) current $I_{\rm PV2}$; (e) power $P_{\rm PV1}$; (f) power $P_{\rm PV2}$; (g) resultant modulation index m_a; (h) output power $P_{\rm OUT}$; (i) modified reference wave $v_{\rm ref\_modified}$; and (j) inverter output voltage $v_{\rm ab}$.

proposed five-level CMLI configuration. Table III gives the value of various parameters used for simulating the proposed five-level CMLI. The proposed five-level CMLI needs to generate a voltage $V_{\rm inv}$ having a phase $\delta_{\rm inv}$ [16] to feed the required amount of active power P into the grid

$$\delta_{\rm inv} = \arctan\left(\frac{2\Pi f_{\rm ac}\left(L_{\rm ac}+L_i\right)P}{v_{\rm ac}^2+R_{\rm ac}P}\right) \tag{22}$$

$$V_{\rm inv} = \left(v_{\rm ac}+\frac{R_{\rm ac}P}{v_{\rm ac}}\right)\frac{1}{\cos\delta_{\rm inv}}. \tag{23}$$

For a power of $P = 2.5$ kW, the value of $\delta_{\rm inv} = 0.117$ rad and $V_{\rm inv} = 323$ V is calculated by substituting the parameters from Table III in (22) and (23), respectively. The simulation waveforms of the proposed five-level CMLI using the proposed PWM technique are shown in Fig. 8. Fig. 8(a) shows the output voltage of the five-level CMLI. The presence of the zero voltage state in all the voltage transitions of $v_{\rm uv}$ can be clearly noticed from the plot. The grid current $i_{\rm ac}$ is shown in Fig. 8(b). The grid current is nearly sinusoidal. The total harmonic distortion of grid current $i_{\rm ac}$ is around 1.76% and meets the requirement of standard IEEE 1547.

The waveform of terminal voltages $v_{\rm xg}$, $v_{\rm yg}$, and $v_{\rm zg}$ are shown in subplots (c), (d), and (e) of Fig. 8, respectively. The crucial observation made from these subplots is the absence of high-frequency voltage transitions. Also, these waveforms match with the result obtained using the switching function analysis (see Fig. 7). This justifies the analysis given in the previous section. Fig. 8(f) shows the waveform for leakage current $i_{\rm leak}$ flowing through the parasitic capacitor. The proposed PWM technique reduces the value of leakage current as can be observed in Fig. 8(f). This is because of the low-frequency voltage transitions in the terminal voltages $v_{\rm xg}$, $v_{\rm yg}$, and $v_{\rm zg}$. The spikes in the leakage current are observed when there is a sudden voltage transition in the terminal voltage. The rms value of $i_{\rm leak}$ is less than 20 mA which is as per the standard VDE0126-1-1 [13]. Fig. 8(g) shows the waveform of CMV $v_{\rm cm}$. The high-frequency voltage transitions in the CMV are also avoided. This further brings down the size, weight, and cost of the electromagnetic interference (EMI) filter to be used in the grid-connected system [22].

Another simulation is carried out with the proposed configuration to demonstrate the MPPT operation. The proposed five-level CMLI is operated using two MPPT algorithms to extract the maximum power from the individual PV arrays. As explained in Section IV, the two individual MPPT algorithms are used for the two PV sources $\rm PV_1$ and $\rm PV_2$ which are identical (having same array configuration). Simulation is done considering a resistive load connected to the output of the inverter via an *LC* filter. The PV modules with an open-circuit voltage of 21.05 V and short-circuit current of 3.74 A at STC are chosen for the array simulation. The electrolytic capacitors of 5000 μF are used as a buffer between the PV sources and inverter as shown in Fig. 1. The inverter is connected to a load of 20 Ω through an *LC* filter with the inductor and capacitor values of 4 mH and 2 μF, respectively. The two PV arrays $\rm PV_1$ and $\rm PV_2$ have an open-circuit voltage of 126.90 V and a short-circuit current of 3.8 A at an insolation of 1.0 sun and the temperature of 50 °C.

Fig. 9 shows the simulation results of MPPT performance for the proposed five-level CMLI. The subplots [see Fig. 9(a) and (b)] show the waveforms of PV voltages $V_{\rm PV1}$ and $V_{\rm PV2}$ for $\rm PV_1$ and $\rm PV_2$ sources, respectively. The values of the operating voltages $V_{\rm PV1}$ and $V_{\rm PV2}$ of the two PV arrays are nearly equal.

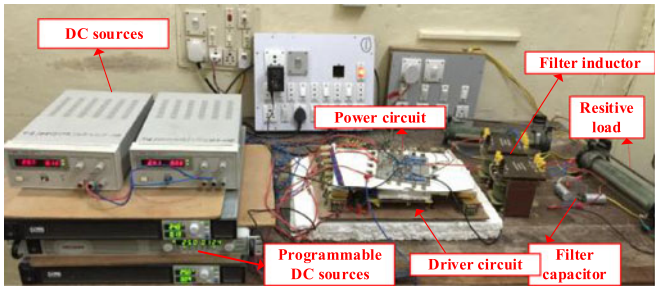

Fig. 10. Photograph of the experimental setup containing five-level and nine-level CMLI.

TABLE IV
PARAMETERS USED FOR EXPERIMENTAL SETUP

Parameter	P	$V_{\rm dc}$	$f_{\rm sw}$	$f_{\rm ac}$	L
Value	54 W	220 V	10 kHz	50 Hz	4 mH
Parameter	C	$R_{\rm load}$	C_p	R_p	
Value	1.25 μF	370 Ω	200 nF	5 Ω	

The PV currents $I_{\rm PV1}$ and I_{PV2} are shown in subplots Fig. 9(c) and (d), respectively. The voltage–current (v-i) characteristics of the PV array can be observed with the increasing value of current by decreasing voltage or vice-versa. The power $P_{\rm PV1}$ and $P_{\rm PV2}$ from the PV sources $\rm PV_1$ and $\rm PV_2$ are shown in subplots Fig. 9(e) and (f), respectively. The operation of two PV sources near MPP can be confirmed with the low value of ripple in the PV power and small oscillations in the modulation index m_a, which can be observed in zoomed part of Fig. 9(g). The waveform of output power across resistive load $P_{\rm load}$ is shown in subplot Fig. 9(h). It can be observed that the power across output load is nearly equal to the sum of the individual PV powers $P_{\rm PV1}$ and $P_{\rm PV2}$. The waveforms of $v_{\rm ref\_modified}$ and $v_{\rm uv}$ are also shown in subplots Fig. 9(i) and (j). Integration of MPPT for the proposed five-level CMLI makes the inverter suitable for the PV systems.

VII. EXPERIMENTAL RESULTS

To validate the analysis and simulation of the PWM technique for the given five-level CMLI, an experimental setup is established. Fig. 10 shows the photograph of the fabricated experimental setup. The details of the parameters used for the experiment are given in Table IV. The MOSFET's with part number IRF840 are employed as switches in the power circuit. The driving pulses for the switches are generated using HCPL 3120. The programmable dc power supplies give the input dc voltage $V_{\rm dc}$ to the inverter [8], [23]–[25] as shown in Fig. 10. The output of the inverter is connected to a resistive load $R_{\rm load}$ through an LC filter. The required PWM pulses are generated using a DIGILENT ATLYS Spartran-6 FPGA board. The frequency of carrier wave $f_{\rm sw}$ and the modified reference wave f_r is selected as 10 kHz and 50 Hz, respectively. The measurement of leakage current is done by connecting a capacitor C_p in series with resistance R_p at point x of the given five-level inverter as shown in Fig. 1.

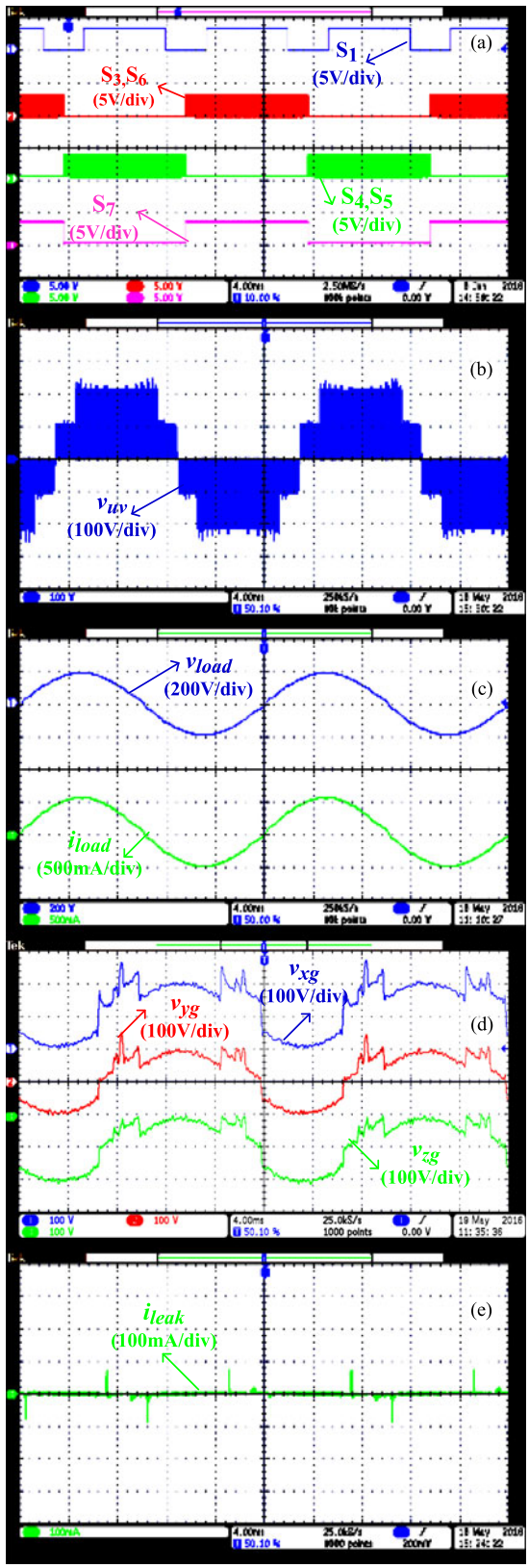

Fig. 11. Experimental waveforms of (a) switching functions of switches S_{x1}, S_{x3}, S_{x4}, S_{x5}, S_{x6}, S_{x7}; (b) output voltage $v_{\rm uv}$; (c) voltage $v_{\rm load}$ across and current $i_{\rm load}$ flowing through resistive load; (d) terminal voltage waveforms of $v_{\rm xg}$, $v_{\rm yg}$ and $v_{\rm zg}$; and (e) leakage current $i_{\rm leak}$ in the parasitic capacitance for the proposed five-level CMLI.

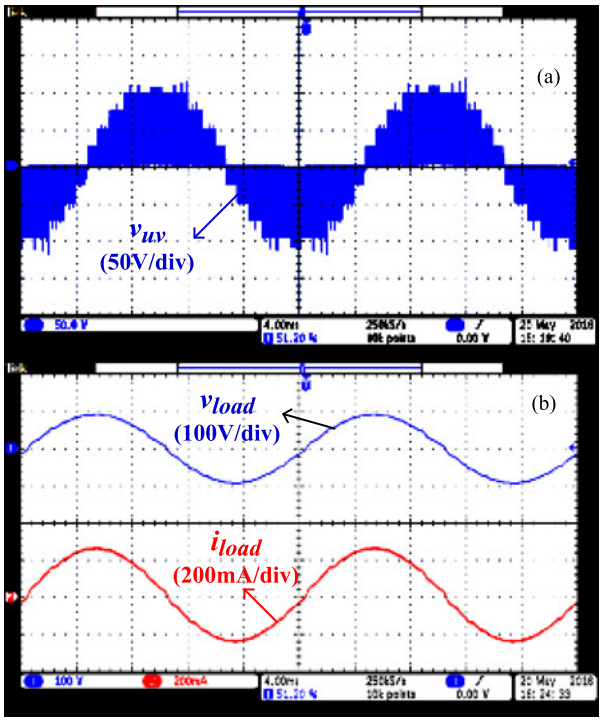

Fig. 12. Experimental waveforms of the nine-level CMLI: (a) output voltage $v_{\rm uv}$; and (b) voltage $v_{\rm load}$ across and current $i_{\rm load}$ flowing through the resistive load.

TABLE V
COMPARISON OF PROPOSED CMLI WITH THE EXISTING TOPOLOGIES

S.No.	Author name [Ref. no.], number of levels in output voltage	A	B	C		D		E		F	
				s	d	p	n	p	n	p	n
1	Zhang *et al.* [9], 3-L	Yes	4	8	–	4	2	2	2	2	2
2	Islam and Mekhilef [10], 3-L	No	2	6	–	3	3	3	3	1	1
3	Xiao *et al.* [11], 3-L	No	2	6	4	2	2	4	4	0	0
4	Ji *et al.* [12], 3-L	No	2	6	2	3	3	2	2	1	1
5	Kerekes *et al.* [23], 3-L	No	3	5	5	2	2	3	3	0	0
6	Islam and Mekhilef [26], 3-L	Yes	2	7	3	2	3	3	3	1	1
7	Wu *et al.* [27], 3-L (HBI MODE)	Yes	4	9	6	6	6	4	4	0	0
8	Wu *et al.* [27], 5-L (CHI MODE)	No	4	8	2	6	6	8	8	0	0
9	Proposed 5-L CMLI	No	2	8	–	3	3	2	2	3	3

A—Asymmetry operation during positive and negative cycle of the MLI.
B—Number of devices conducting in zero voltage state including switches and diodes.
C—Number of devices used in the MLI.
s—Number of switches used in the MLI.
d—Number of diodes used in the MLI.
D—Number of devices including switches and diodes conducting.
p—During the positive half-cycle of the grid voltage.
n—During the negative half-cycle of the grid voltage.
E—Number of switches operating at high switching frequency.
F—Number of switches operating at low switching frequency.

Fig. 11 shows the experimental waveforms of the proposed five-level CMLI. Fig. 11(a) shows the waveform of switching states of switches S_{x1}, S_{x3}, S_{x4}, S_{x5}, S_{x6}, and S_{x7}. The switches (S_{x1}, S_{x2}) and (S_{x7}, S_{x8}) are operated at low switching frequency. The remaining switches (S_{x3}, S_{x6}) and (S_{x4}, S_{x5}) operate only in positive and negative half-cycles of the inverter output voltage $v_{\rm uv}$, respectively. The inverter output voltage $v_{\rm uv}$ is shown in Fig. 11(b). The zero voltage state is present in all the switchings of the inverter output voltage. This may increase the filter inductor value at the output of the MLI. However, the minimization of high-frequency transitions in the terminal voltage reduces EMI filter requirement for the proposed system. The waveforms of the voltage across resistive load $v_{\rm load}$ and the current flowing through the resistive load $i_{\rm load}$ are shown in Fig. 11(c). The waveforms of the terminal voltages $v_{\rm xg}$, $v_{\rm yg}$, and $v_{\rm zg}$ are shown in Fig. 11(d). It may be noted that the terminal voltage is free from high-frequency transitions, which demonstrates the effectiveness of the proposed PWM technique. Fig. 11(e) shows the leakage current $i_{\rm leak}$ flowing through the $C_p - R_p$ branch. The magnitude of leakage current is less than 100 mA and is as per standard VDE0126-1-1.

To demonstrate the upgradability of the proposed topology to any generalized $2m + 1$ level inverter, a hardware prototype for the nine-level CMLI is fabricated. The nine-level configuration of proposed CMLI is obtained by cascading two basic units in generalized configuration with the bidirectional switches as shown in Fig. 4. Fig. 12 shows the experimental waveforms obtained from the developed hardware prototype of the nine-level inverter connected to a resistive load. The parameters shown in Table IV are again used, except the input dc voltage which is reduced to 100 V. Fig. 12(a) shows the waveform of inverter output voltage $v_{\rm uv}$. The nine levels of the inverter output voltage can be clearly observed in the voltage waveform. The presence of the zero voltage state for a complete cycle of the output voltage is also observed from the plot. The waveforms of the voltage across the resistive load $v_{\rm load}$ and the current flowing through resistive load $i_{\rm load}$ are shown in Fig. 12(b).

VIII. COMPARISON OF PROPOSED CMLI WITH THE EXISTING MLI TOPOLOGIES

The proposed five-level CMLI is compared with the existing PV MLI topologies from the literature available. Table V gives the comparison details of the proposed five-level CMLI with the existing PV MLI topologies. It can be observed that the other topologies (see Table V) require almost the same number of devices for the generation of three levels in the output voltage. The proposed CMLI also requires nearly the same number of semiconductor devices for the generation of five levels in the inverter output voltage. Hence, the proposed five-level CMLI is economical. Furthermore, the proposed five-level CMLI have reduced switching and conduction losses. The other existing topologies shown in Table V have either high switching loss or conduction loss. The problem of asymmetry in the output voltage of the inverter is also avoided in the proposed CMLI topology. Also, the number of devices conducting during zero voltage state always remains two. Thus, the proposed CMLI is expected to show high efficiency. To support the efficient operation of the proposed CMLI, loss calculation (switching and

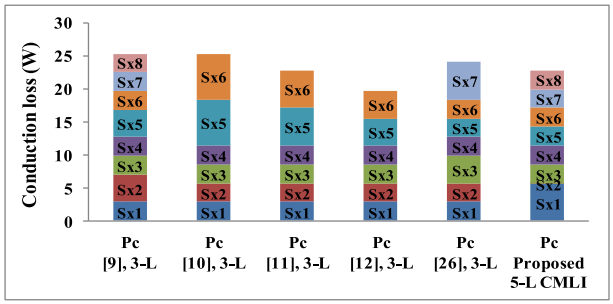

Fig. 13. Value of conduction losses P_c of switches used in various MLI topologies given in the literature.

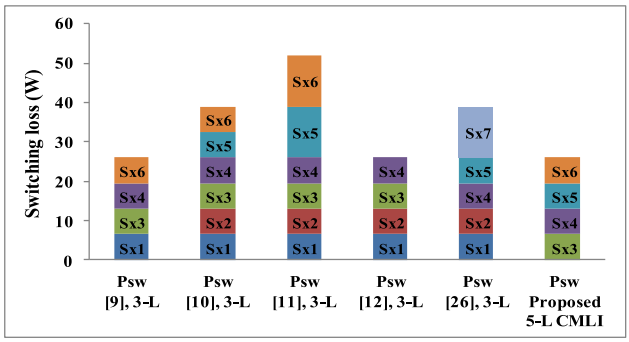

Fig. 14. Value of switching loss $P_{\rm sw}$ of switches used in various MLI topologies presented in the literature.

conduction losses) for the controlled switching devices is done under identical conditions. The losses in other MLI topologies are also calculated under the same conditions of output power $P = 2.5$ kW, switching frequency $f_{\rm sw} = 25$ kHz, $V_{\rm dc} = 400$ V, and $m_a = 0.8125$. The expressions for switching and conduction losses used for the calculation are obtained from [12] and [28]. Figs. 13 and 14 show the calculated value of conduction and switching losses in the form of bar charts for various MLI topologies reported in the literature. Furthermore, in Figs. 13 and 14, the terms P_c and $P_{\rm sw}$ refer to the conduction and switching losses, respectively, for each of the MLI topologies reported in the literature. Conduction and switching losses of the individual switches in each MLI topology are shown in different color blocks in the bar chart of P_c and $P_{\rm sw}$, respectively. It can be observed that the proposed five-level CMLI shows higher efficiency compared to the other existing topologies. Hence, the proposed five-level CMLI is efficient and economical.

IX. Conclusion

In this paper, an improved five-level CMLI with low switch count for the minimization of leakage current in a transformerless PV system was proposed. The proposed CMLI minimized the leakage current by eliminating the high-frequency transitions in the terminal and CMVs. The proposed topology also reduced conduction and switching losses which made it possible to operate the CMLI at high switching frequency. Furthermore, the solution for generalized $2m + 1$ levels CMLI was also presented in the paper. The given PWM technique required only one carrier wave for the generation of $2m + 1$ levels. The operation, analysis of terminal, and CMVs for the CMLI were also presented in the paper. The simulation and experimental results validated the analysis carried out in this paper. The MPPT algorithm was also integrated with the proposed five-level CMLI to extract the maximum power from the PV panels. The proposed CMLI was also compared with the other existing MLI topologies in Table V to show its advantages.

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